Sapienza PhD in ICT

Doctoral program in Information and Communications Technologies at Sapienza Università di Roma, Rome, Italy

Second Year Doctoral Program Form

LAST NAME	BLASI
NAME	LUIGI
CURRICULUM	ELECTRONIC ENGINEERING
DOCTORAL CYCLE	XXXIII CYCLE

The Doctoral Program Form contains, year by year, the description of the PhD program of each Doctoral student. This form must be submitted to the PhD coordinator with roughly the following timing:

- by the end of February of the first year for first year students
- by the end of December of the second year by second year students
- by the end of December of the third year by third year students

The Doctoral Program Proposal is approved by the PhD board shortly after submission.

The Doctoral Program requirements place formalized emphasis on methodology and mastery of fundamental and applied engineering systems concepts. A Doctoral Program Proposal should be constructed in agreement with the Faculty mentor, that is the supervisor or tutor, by complying to the requirements, described in the Tables below.

ADVANCED COURSES: 0 CREDIT FORMATION UNITS (CFU)[1][2]
Only courses/schools providing a final verification test with pass/fail outcome certified by instructor can be included here.

Title	Type	Duration / period	CFU[3]	Motivation for selection
Machine Learning for Signal Processing	Master Degree course	September-December 2019	6	This course is focused on Machine Learning signal processing techniques which are gaining popularity nowadays in all those application fields which require an adaptive and dynamic response to all the systems changes.
Total CFU			6	

SEMINARS AND LABORATORY ACTIVITIES: 6 CFU[4]

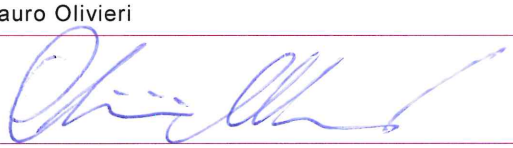
Activity	Type	Duration / period	CFU[5]	Motivation for selection
Laboratorio di Elaborazione Multimediale	Master Degree course	September-December 2019	6	This course is focused on the MATLAB programming techniques which are useful for 1D 2D and 3D data.
Total CFU			6	

ADDITIONAL INDEPENDENT FORMATION AND RESEARCH ACTIVITIES: 6 CFU[6]
Indicate activities that extend and complement the mandatory activities listed above

[1] Please insert lines as required/appropriate, and for each line complete each column of the Table.
[2] During the second year, the doctoral student may complete the credits corresponding to advanced courses that were not completed in the first year.
[3] Indicate here the CFUs that can be accounted for as a result of the successful completion of the activity; for Master Degree courses, assume 1 CFU = 8 teaching hours + 12 homework/study hours, for a total of 20 hours. This rule can be slightly adjusted for other types of courses/activities (e.g., PhD courses may require slightly less hours per CFU)
[4] Please insert lines as required/appropriate, and for each line complete each column of the Table.
[5] Indicate here the CFUs that can be accounted for as a result of the successful completion of the activity; as a rule of thumb, assume 1 CFU = 20 working hours.
[6] Please insert lines as required/appropriate, and for each line complete each column of the Table.

Activity	Type	Duration / period	CFU[7]	Motivation for selection
RISC-V 2019 Workshop (Zurich, Switzerland)	Workshop	11-13th June	2	Preparation and presentation of a 15 minute session *"The first space-qualified Klessydra RISC-V microcontroller to be launched on a satellite"*
Digital System Lab meetings (Rome)	Meeting	-	> 3	Planning and definition of the Klessydra Orbital Lab Platform which will be used as a secondary payload within Pocket Cubesat.
APPLEPIES 2019 International Conference (Pisa)	Conference	September 12-13 2019	1	Preparation of the conference paper *"A RISC-V Fault-Tolerant Microcontroller Core Architecture Based on a Hardware Thread Full-Weak protection and a Thread-Controlled Watch-Dog Timer"*
Total CFU				

RESEARCH ACTIVITY: 42 CFU	
Research area	Multi-level design of resilient digital system for safety critical applications, in particular avionics, aerospace, railways, automotive and wearable devices for critical work environments (such as contaminated/polluted environments, burned areas and radioactive zones)
Research topic	The aim of the research activity is focused on implementation and evaluation of several RISC-V compatible microcontroller core architectures for space-qualified fault-tolerant microcontroller cores which supports natively interleaved multithreading.
Framework of the proposed research topic	The first step will be the definition of a new metric to evaluate fault-tolerance of a microcontroller core microarchitecture ion as well as a benchmark set. This will be followed by a deep study activity based on the state-of-art radiation hardening techniques which are used to mitigate the ionizing radiation effects on FPGAs, ASICs and Microprocessors. The second step will be the study of the state-of-the-art RISC-V microcontroller cores architectures currently available and the definition of a new set of architectures which will be implemented. The third step will be the HDL implementation and verification compared to the metrics defined in the first step.
Research environment	Digital System Lab at Sapienza (prof. Olivieri) Collaboration with Dept. of Aerospace Engineering (prof. Nascetti)

FACULTY MENTOR (TUTOR OR SUPERVISOR)	
Prof. Dr.	Mauro Olivieri
Supervisor signature for approval	

Signature of Doctoral student Date

[7] Indicate here the CFUs that can be accounted for as a result of the successful completion of the activity; as a rule of thumb, assume 1 CFU = 20 working hours.