Sapienza PhD in ICT

Doctoral program in Information and Communications Technologies at Sapienza Università di Roma, Rome, Italy

First Year Doctoral Program Form

LAST NAME	**BLASI**
NAME	**LUIGI**
CURRICULUM	**ELECTRONIC ENGINEERING**
DOCTORAL CYCLE	**XXXIII CYCLE**

The Doctoral Program Form contains, year by year, the description of the PhD program of each Doctoral student. This form must be submitted to the PhD coordinator with roughly the following timing:

- by the end of February of the first year for first year students
- before the admission to the second year by perspective second year students
- before the admission to the third year by perspective third year students

The Doctoral Program Proposal is approved by the PhD board shortly after submission. The Doctoral Program requirements place formalized emphasis on methodology and mastery of fundamental and applied engineering systems concepts. A Doctoral Program Proposal should be constructed in agreement with the Faculty mentor, that is the supervisor or tutor, by complying to the requirements, described in the Tables below.

ADVANCED COURSES: 12 CREDIT FORMATION UNITS (CFU)[1]
Only courses/schools providing a final verification test with pass/fail outcome certified by instructor can be included here.

Title	Type	Duration / period	CFU[2]	Motivation for selection
Digital System Programming	Master Degree course	March-May 2018	6	This course is focused on microcontrollers and microprocessor programming using C/C++ languages as well as Linux OS Bourne Again Shell scripting. It's useful to improve my basic knowledge in such programming techniques and environments which are mandatory for an electronic engineer.
Machine Learning for Signal Processing	Master Degree course	March-May 2018	6	This course is focused on Machine Learning signal processing techniques which are gaining popularity nowadays in all those application fields which require an adaptive and dynamic response to all the systems changes.
Total CFU			12	

SEMINARS AND LABORATORY ACTIVITIES: 6 CFU[3]

Activity	Type	Duration / period	CFU[4]	Motivation for selection
4th IAA Conference on University Satellite Missions and CubeSat Workshop	Conference and Workshop	4th December – 7th December	1	Insert here a detailed explanation of why the activity was selected and included in the doctoral program, and how it connects with the research area of the PhD student.
TOP IMPALART linear accelerator ground test at Centro Ricerche Frascati - ENEA	Laboratory	March – June 2018	1	This activity will test the radiation hardening capability of a custom FPGA microcontroller soft-IP core using electrons and protons particles beams generated by a linear accelerator. They will be performed using TOP IMPALART linear particles accelerator at Centro Ricerche Frascati – ENEA

[1] Please insert lines as required/appropriate, and for each line complete each column of the Table.
[2] Indicate here the CFUs that can be accounted for as a result of the successful completion of the activity; for Master Degree courses, assume 1 CFU = 8 teaching hours + 12 homework/study hours, for a total of 20 hours. This rule can be slightly adjusted for other types of courses/activities (e.g., PhD courses may require slightly less hours per CFU)
[3] Please insert lines as required/appropriate, and for each line complete each column of the Table.
[4] Indicate here the CFUs that can be accounted for as a result of the successful completion of the activity; as a rule of thumb, assume 1 CFU = 20 working hours.

Laboratorio di Elaborazione Multimediale	Master Degree course	March – May 2018	6	This course is focused on the MATLAB programming techniques which are useful for 1D 2D and 3D data.
Total CFU			8	

ADDITIONAL INDEPENDENT FORMATION AND RESEARCH ACTIVITIES: 6 CFU[5] Indicate activities that extend and complement the mandatory activities listed above				
Activity	**Type**	**Duration / period**	**CFU[6]**	**Motivation for selection**
Learn Vivado from Top to Bottom – The Complete Guide FPGAs design with HLS (High Level Syntesis Tool) Electrical, Electronics and PCB Design Safety & Compliance	UDEMY Online Training Course	January – September 2018	1	This course Is focused on the Xilinx Vivado Ide which is nowadays a standard development IDE for FPGAs design (4.5 hours) This course Is focused on the Xilinx Vivado HLS (High Level Syntesis) which is an alternative to the standard FPGA design flow using VHDL or VERILOG hardware description languages (2 hours) This course is focused on the most important aspects and methods for designing safe electrical and electronics products and applications (3 hours)
Learn to Design your own board with ALTIUM designer	UDEMY Online Training Course	January – September 2018	1.5	This course is focused on digital/analog hardware board design using the ALTIUM PCB designer tool (15 hours)
Mastering RTOS	UDEMY Online Training Course	January – September 2018	1.5	This course is focused on Real-time operating systems using FreeRTOS, Arduino boards, STM32F4x and ARM cortex M based Mircocontrollers (16hours)
Mastering Microcontroller with Embedded Driver Development	UDEMY Online Training Course	January – September 2018	2	This course is focused on microcontrollers embedded driver development using C/C++ language (18h)
QT C++ GUI Tutorial For Beginners	UDEMY Online Training Course	January September 2018	1	This course is focused on C++ graphical user interface design using the Qt framework (9hours)
Total CFU			6	

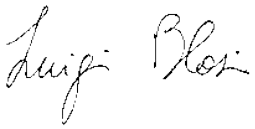
RESEARCH ACTIVITY: 36 CFU	
Research area	Multi-level design of resilient digital system for safety critical applications, in particular avionics, aerospace, railways, automotive and wearable devices for critical work environments (such as contaminated/polluted environments, burned areas and radioactive zones)
Research topic	The aim of the research activity is to study and define new digital hardware systems design techniques using several abstraction levels (circuit-level, gate-level, register-transfer-level, embedded system level, OS level and application SW level) in order to improve the overall system resilience performance. In particular the HW and SW architectures which are used to enhance the system resilience with respect to the ionizing radiation damages (e.g. aerospace, avionics and nuclear power plant systems) will be emphasized.
Framework of the proposed research topic	The first step will be the definition of a new metric to evaluate resilience performance of a safety critical system as well as an application benchmark set. This will be followed by a deep study activity based on the state-of-art radiation hardening techniques which are used to mitigate the ionizing radiation effects on FPGAs, ASICs and Microprocessors. The second step will be a ground test and detailed analysis of the ionizing radiation effects induced by a particle electrons and protons beams on a microcontroller FPGA design. At the same time a new hardening design techniques will be studied and implemented on a custom RISC V microprocessor (KLESSYDRA) taking into account all the previous acquired knowledge and experiments results.
Research environment	Collaboration with Centro Nazionale Ricerche Frascati – ENEA (Ing. Paolo Nenzi)

FACULTY MENTOR (TUTOR OR SUPERVISOR)	
Prof. Dr.	Mauro Olivieri

[5] Please insert lines as required/appropriate, and for each line complete each column of the Table.
[6] Indicate here the CFUs that can be accounted for as a result of the successful completion of the activity; as a rule of thumb, assume 1 CFU = 20 working hours.

Supervisor signature for approval	

Signature of Doctoral student



Date

23/03/2018